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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/660,439	09/12/2000	Toshiyuki Takemori	001155	6603

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EXAMINER
RAO, SHRINIVAS H

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/660,439	Applicant(s) TAKEMORI ET AL.	
	Examiner Steven H. Rao	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 16-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-11 and 16-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 35 U.S.C. Section 132 and 37 CFR 1.114 claiming priority from U.S. Serial No. 09/660,439 which itself claims priority under 35 U.S.C. Section 119(a)-(d), from Japanese Patent Application No. Hei 11-258687 filed on 13/9/1999, which papers have been placed of record in the file.

Continued Prosecution Application

The request filed on 9/8/2000 for a request for Continued Application (RCE) under 37 CFR 1.114 based on parent Application No. 09/660,439 is acceptable and a RCE has been established. An action on the RCE follows.

Preliminary Amendment Status

Acknowledgment is made of entry of preliminary amendment filed 3 /13 /03. Therefore claims 1 and 11 as amended by the amendment, claims 2-10,17-19 as previously recited and presently newly added claims 21-22 are currently pending in the application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11 and 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baliga (U.S. Patent No. 5,98,833 herein after Baliga) and Sapp (U.S. Patent No. 6,351,018, herein after Sapp) both previously applied and further in view of Jarred (G.B Patent No. 2,347, 014, herein after Jarred) newly applied.

With respect to claims 1 and 11, Baliga describes a transistor including: a semiconductor substrate having a semiconductor layer (Fig. 2, col. 3 line 7), a drain layer provided on the semiconductor layer (fig.2 # 1'14, col. 3 line 7), and an oppositely conductive region of a second conductivity type provided on the drain layer fig.2 # 112, col. 3 lines 12-15) and a trench extending from a surface of the opposite conductivity region to the drain region (fig.2 # area bounded by 120 a and 120b, col. 3 lines 33-40), a source region of the first conductivity type provided in the oppositely conductive region and exposed on an inner circumferential surface of the trench (fig.2 #126 or fig. 3 # 128a, col. 3 line 39 and col. 7 line 41-42), a gate insulating film provided on the inner circumferential surface and inner bottom surface of the trench such that it reaches to the drain layer, the oppositely conductive region and the source region.

Baliga does not specifically describe its gate insulating film provided on the inner circumferential surface and inner bottom surface of the trench such that it reaches to the drain layer.

However, Sapp in fig. 2 and col. 2 lines 33-45 describes a bottom part of the insulating layer being in contact with upper part of drain region (col.2 line 43-45) to provide isolation trenches that allow large anode contact area that connects to the trench MOSFET source terminal thus resulting in better devices.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Sapp's gate insulating film having its bottom part being in contact with upper part of drain region in Baliga's device to provide isolation trenchs that allow large anode contact area that connects to the trench MO1>FET source terminal thus resulting in better devices. (Sapp col. 4 lines 60-65).

The other limitations of claim1 are:

a gate electrode material provided in tight contact with the gate insulating film (Baliga fig. 2 # 126 in contact with 124, col. 3 lines 37-40 and fig. 3 # 128 a in contact with 125, col. 7 lines 40-45), a source electrode film provided in contact with at least the source region exposed at least on the side surface of said trench and electrically insulated from the gate electrode material (fig.2 # 118 col. 3 lines 45-50 and fig. 3 # 128b col. 6 lines 51-56) and source region being substantially square when viewed from a direction parallel to said side surface of said trench, (Baliga figure 2) said source electrode film being contiguous and extending from an upper portion of said source region

Baliga does not specifically describe the source electrode extending on a side surface of said source region .

However Jarred in figure 2 and page 6 lines 4 to 11 describes the source electrode extending on a side surface of said source region to control the total area of contact between the source region and the source conductor is a known quantity thereby very accurate channel width definition is possible and also diffusion distances can be very much reduced.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Jarred's source electrode extending on a side surface of said source region in Baliga and Sapp's devices to control the total area of contact between the source region and the source conductor is a known quantity thereby very accurate channel width definition is possible and also diffusion distances can be very much reduced. (Jarred page 2 2para , page 3 3rd para and page 4 1 st para).

The last limitation of claim1 is ;

said contiguous source electrode film covering an opening of said trench in its entirety. (Baliga figure 3, Jarred fig. 2).

Claim recites the further element a metal film formed on a surface of said drain layer opposite to said conductive region to establish Schottky contact with said drain layer. (Baliga col. 11 lines 14-19).

With respect to claim 2, wherein a drain electrode formed on a surface of the semiconductor layer opposite the drain layer (fig. 2,3 # 116 , col. 3 line 47 and col. 7 lines 1-10).

With respect to claim 3, wherein the impurity concentration of the semiconductor layer is higher than the impurity concentration of the drain layer (col. 8 line 65 to col. 9 line 21).

With respect to claims 4 to 7, wherein the insulating material thicker than the gate insulating film is provided between the gate electrode material in the trench and the source electrode film. (figs. 4H # 30, col. 10 lines 10-14),

With respect to claim 8, wherein the trench has a mesh on the top surface and the source region is provided in contact with the trench (figs. 3 and 4).

With respect to claims 9 and 10, wherein the semiconductor layer is of the first conductivity type or second conductivity type in relation to the opposite type drain layer (col. 6 lines 35-40). With respect to claim 11,to the extent understood, Baliga describes a transistor including

'With respect to claims 16 and 18, to the extent understood, it repeats the elements of claims 1 and 11 and adds that the transistor comprises a plurality of source regions (Baliga figs. 4C-K, col. 9 lines 25-26) is rejected for reasons stated above and incorporated here by reference.

With respect to claims17 and 19, wherein the when each of the source regions is annular when viewed from a direction parallel to said side surface of said trench. (Sapp fig.2 col. 3 lines 58-62).

.Claims 20 and 21 repeat the same elements of claims 1 and 11 respectively and are rejected for reasons stated above.

Claims 20 and 21 further recite a plurality of trenches (instead of a trench) (Sapp figs 2-4 or Jarred figure 2) and also the contiguous source electrode film covering a plurality of opening of said trenches in their entireties (Jarred fig.2 # 8 covering the trenches in their entireties.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Steven H. Rao

Patent Examiner

May 29, 2003.

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800